

09/164,216

Response to Office Action Mailed December 17, 2002

TH  
cont'd. J1

a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

---

#2  
J1

51. (Twice Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:  
a plurality of pads;  
an electrostatic discharge (ESD) negative ring;  
a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;  
a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate;  
a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring; and  
a plurality of second diodes connected to the pads so that each second diode is connected to a pad and a positive line.

---

52. (Twice Amended) The chip of claim 51 wherein the switch blocks a current from flowing from the positive line to the negative ring when a voltage on the positive line rises at a second rate that is different from the first rate.

53. (Twice Amended) The chip of claim 51 wherein a second diode is forward biased when the voltage on the positive line rises at the second rate.

---

#3  
J1

56. (Amended) The chip of claim 51 wherein an ESD switch is directly connected to a positive line and the negative ring.

09/164,216  
Response to Office Action Mailed December 17, 2002

#3  
cont'd.  
J1

57. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:  
a plurality of pads;  
an electrostatic discharge (ESD) negative ring;  
a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other, none of the positive lines being directly connected to a pad;  
a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring;  
a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and  
a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

#4 J1

60. (Amended) The semiconductor chip of claim 57 wherein an ESD switch is directly connected to a positive line and the negative ring.

#5 J1

62. (Amended) A semiconductor chip having a substrate of a first conductivity type, the chip comprising:  
a plurality of pads;  
an electrostatic discharge (ESD) negative ring;  
a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;  
a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each ESD switch is connected to a positive line and the ESD negative ring, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate that is faster than a second rate;  
a plurality of first diodes connected so that each first diode is connected between a pad and the negative ring; and

09/164,216

Response to Office Action Mailed December 17, 2002

#5 J1  
could. a plurality of second diodes connected so that each second diode is connected between a pad and a positive line.

#6 J1 65. (Amended) The semiconductor chip of claim 62 wherein an ESD switch is directly connected to a positive line and the negative ring.

Please add the following new claims:

#7 J1 --67. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that only one second diode is connected between a pad and a positive line.

09/164,216  
Response to Office Action Mailed December 17, 2002

68. A semiconductor chip having a substrate of a first conductivity type, the chip comprising:

a plurality of pads;

an electrostatic discharge (ESD) negative ring;

a plurality of ESD positive lines, the plurality of positive lines not being electrically connected to each other;

a plurality of ESD switches connected to the ESD positive lines and the ESD negative ring so that each positive line is connected to the negative ring via an ESD switch, a switch of the plurality of ESD switches passing a current from a positive line to the negative ring when a voltage on the positive line rises at a first rate;

a plurality of first diodes connected to the pads so that each first diode is connected to a pad and the negative ring, a first diode of the plurality of first diodes comprising:

a plurality of first regions, the plurality of first regions being spaced apart from each other;

a second region, the plurality of first regions being formed in the second region, the plurality of first regions and the second region having opposite conductivity types, the second region having a dopant concentration; and

a third region formed in the second region, the third region being spaced apart from each first region, and formed between each adjacent pair of first regions, the third region having a dopant concentration that is higher than the dopant concentration of the second region; and

a plurality of second diodes connected to the pads so that only one second diode is connected between each pad and each positive line.

69. The chip of claim 15 wherein a second diode is directly connected to a pad and directly connected to a positive line.

09/164,216

Response to Office Action Mailed December 17, 2002

70. The chip of claim 57 wherein a second diode is directly connected to a pad and directly connected to a positive line.

71. The chip of claim 51 wherein a second diode is directly connected to a pad and directly connected to a positive line.

72. The chip of claim 62 wherein a second diode is directly connected to a pad and directly connected to a positive line.--